REMARKS

Claims 1-15, 17, 18, 20, and 22-32 are presented for further examination. Claims 1, 6, 10, 11, 17, 18, and 20 have been amended. Claims 16, 19, and 21 have been canceled, and claims 29-32 are newly presented.

In the Office Action mailed May 27, 2004, the Examiner objected to claim 6 because "a stack of modules" should be -- the stack of modules --. Applicant has so amended the claim, and thereby requests withdrawal of the rejection.

Claims 1-3, 6-8, 10-14, and 16-17 were rejected under 35 U.S.C. § 102(b)-(e) as anticipated by U.S. Patent No. 6,477,593 ("Khosrowpour et al."). Claims 9, 15, and 18 were rejected as anticipated by U.S. Patent No. 6,109,929 ("Jasper"), and claim 19 was rejected as anticipated by U.S. Patent No. 6,431,879 ("Brekosky et al."). In addition, the Examiner has rejected claims 20-22 and 24-27 under 35 U.S.C. § 103(a) as obvious over Khosrowpour et al., claims 4 and 28 as obvious over Jasper, and claims 5 and 23 as obvious over the combination of Khosrowpour et al. and Brekosky et al.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

Claim 1, as now amended, recites a stackable module for a processor system that includes, *inter alia*, a topside connector mounted to the topside of a support plate, and an underside connector mounted to the underside of the support plate directly under and corresponding to the topside connector. Claim 1 further recites a first set of conductive tracks connected directly between the topside connector and the corresponding underside connector, and a second set of conductive tracks connecting the topside connector to a set of topside circuit components.

Claim 1 is distinct over Khosrowpour et al. because of the nature of the connections of the conductive tracks arranged to convey the transport stream. More particularly, claim 1 recites the first set of conductive tracks connected directly between the topside connector and the corresponding underside connector. Khosrowpour et al. teach that busses do not pass directly between the connectors, but cross over to a different connector on the top or underside of each module. This is because Khosrowpour et al. specifically teach "alternating connectivity is provided between the VO bridge circuits 124, 134 and the first and second busses 114A, 114B of

the motherboard 110" to enable connection of the daughter board in any position. (*See* Khosrowpour et al., column 4, lines 60-63 and claims 1 and 12 thereof.)

Furthermore, claim 1 of the present invention recites "a second set of conductive tracks connecting the topside connector to the set of topside circuit components." In Khosrowpour et al. there is no teaching or suggestion that the connection between the data bus provided by the lower connector (*e.g.*, 122D) and the corresponding circuit (I/O bridge circuit 124) is anything other than a direct connection and not a second set of conductive tracks.

In view of the foregoing, applicant respectfully submits that claim 1 and dependent claims 2-9, as well as independent claims 10 and 11 and corresponding dependent claims 12-15 are allowable.

Independent claim 17 is directed to a stackable module for a processor system, the module comprising substantially all of the elements of claim 1 and further including a "multiplexer for selectively selecting the transport stream data from a lower module in the stack and an upper module in the stack for acting on by a device mounted on the topside of a support plate." New claim 29 includes the feature of "a multiplexer for selectively selecting the transport stream data from a lower module in the stack and an upper module in the stack for action on by said device." This feature is also recited in dependent claims 8, 14, and 27. The Examiner has asserted that this feature is anticipated by Khosrowpour et al. Applicant respectfully disagrees.

Applicant can find no teaching or suggestion in Khosrowpour et al. of the use of multiplexers in the module in order to select data that is input to the module. In particular, in the present invention the multiplexer can be used to select a transport stream that is input to the module from either lower down the stack or higher up the stack. No similar functionality is disclosed in Khosrowpour et al. Rather, Khosrowpour et al. disclose only the features of the busses crossing over each other as they pass through the module (*see* Figure 3 of Khosrowpour et al.). This feature means that the bus that is inputted to the module can be selected through its position in the stack (*i.e.*, a module that has an odd number of modules below it in the stack will be connected to one bus and an even number will be connected to the other). However, this structure taught by Khosrowpour et al. lacks many of the advantages of flexibility that the present invention provides through the use of a multiplexer.

The Examiner has stated, with respect to claims 8 and 14, that the circuit components of Khosrowpour et al. "can act" as a multiplexer. However, it is clearly shown in Figure 3 of Khosrowpour et al. that only one input line is present to the circuit in each module. Therefore, even if the circuitry were able to operate as a multiplexer (of which there is no suggestion), it could not do so in the same manner as recited in the claims of the present invention. Thus, applicant submits that claim 17, as well as new independent claim 29, and dependent claims 8, 14, and 27 are allowable for these reasons.

Claim 18 and new independent claim 30 are directed to the feature that "the circuit components constitute a device that does not utilize the transport stream data and the transport stream control signals, all of the transport stream data and the transport stream control signals being supplied via the top side and underside connectors directly to another module in a stack of modules." This feature is also recited in dependent claims 9, 15, and 28.

The Examiner has asserted that Jasper anticipates this feature. However, Jasper teaches a memory module system that does not utilize, teach, or suggest this feature. More particularly, the connections of Jasper are not used for conveying transport stream data. Rather, they are used for memory access operations from the processor. Even if the connections are taken as analogous, then it is clear that Jasper does not teach or suggest the claimed feature. As can be seen in Figure 4A of Jasper, each of the circuit elements on the modules are wired directly to the connectors, and thus to the processor. None of the circuits in Jasper have elements that do not use the data connection. In fact, it would be pointless for Jasper to teach or suggest providing a module that passes the data to the module above without interacting with it because only memory modules are disclosed, and these would be useless without a direct connection to the processor. Hence, applicant submits that claim 8 as well as dependent claims 9, 15, and 28 are allowable.

New independent claims 31 and 32 recite the feature of "wherein each of the topside and underside connectors comprises a set of pins for carrying memory access signals to enable the module to function as an external memory interface." This feature is found in dependent claim 2 and in former dependent claim 21, which has now been incorporated into independent claim 20 from which dependent claims 22-28 all ultimately depend.

The Examiner has asserted that this feature is taught by Khosrowpour et al. However, Khosrowpour et al. make no mention of providing memory access functionality in the modules. Rather, Khosrowpour et al. only disclose using the modules to bridge between different types of data bus (*e.g.*, PCI bus to Fibre Channel). Khosrowpour et al. only teach the first bus being inputted to the module and a second bus type being outputted. There is no teaching or suggestion in Khosrowpour et al. of further pins being included in the module connectors, in addition to the data bus, to allow another type of module that provides memory access to be utilized. Hence, applicant submits that claims 2, 20-28, 31, and 32 are clearly allowable.

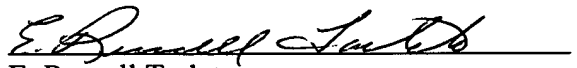
Applicant is submitting herewith a Terminal Disclaimer to overcome the double patenting rejection.

In view of the foregoing, applicant submits that all of the claims remaining in this application are clearly in condition for allowance. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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